

CLAIM AMENDMENTS

This listing of claims will replace all prior versions and listings of claims in the application.

1 1. (Currently Amended) A multimedia data processing system, comprising:

2 a first integrated circuit, the first integrated circuit comprising:

3 a first logic block generating a receiving an encoded multimedia data

4 stream;

5 a hardware encryption circuit coupled to the first logic block, the

6 hardware encryption circuit encrypting the received data stream to generate

7 an encrypted data stream with access control; and

8 a first Peripheral Component Interconnect Express (PCI-Express) -

9 compatible interface circuit supporting data communication over a plurality

10 of PCI-Express virtual channels, wherein the plurality of PCI-Express virtual

11 channels comprises at least an unencrypted default virtual channel and a

12 dedicated encrypted virtual channel, wherein the first PCI-Express-

13 compatible interface circuit includes a first plurality of channel interconnects,

14 each channel interconnect associated with a virtual channel among the

15 plurality of virtual channels, wherein a first channel interconnect among the

16 plurality of virtual channels is coupled to the hardware encryption circuit to

17 receive the encrypted data stream, and wherein the first PCI-Express-
18 compatible interface circuit communicates the encrypted data stream from
19 the hardware encryption circuit over the dedicated encrypted virtual channel;
20 a second integrated circuit coupled to the first integrated circuit by a PCI-
21 Express-compatible interconnect, the second integrated circuit comprising:

22 a second PCI-Express-compatible interface circuit coupled to the PCI-
23 Express-compatible interconnect to receive the encrypted data stream over
24 the dedicated encrypted virtual channel, the second PCI-Express-compatible
25 interface circuit comprising:

26 a second plurality of channel interconnects, each channel
27 interconnect associated with a virtual channel among the plurality of
28 virtual channels;

29 a hardware decryption circuit coupled to a first channel
30 interconnect among the second plurality of channel interconnects for
31 the second PCI-Express-compatible interface circuit and configured to
32 decrypt the encrypted data stream; and

33 a second logic block coupled to the hardware decryption circuit
34 and configured to use decoding the decrypted data stream, the
35 decoding providing the multimedia stream to a subscriber authorized
36 by the access control; and

37 control logic coupled to at least one of the first and second PCI-Express-
38 compatible interface circuits and configured to communicate authorization data
39 over the default virtual channel to authorize secure communication between the
40 first and second integrated circuits over the dedicated encrypted virtual channel,
41 wherein all data sent over the dedicated encrypted virtual channel are encrypted;
42 ~~and access-control-and-decoding-are-separately-performed-on-the-first-and-second~~
43 ~~integrated-circuits-for-the-dedicated-encrypted-virtual-channel.~~

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1 2-3. (Canceled).

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1 4. (Currently Amended) The ~~circuit arrangement of claim 2~~ ~~system of claim 1,~~
2 ~~further comprising: wherein the first~~ ~~[[a]]~~ logic block ~~coupled to the hardware~~
3 ~~encryption circuit and configured to output~~ ~~outputs the multimedia data stream~~ for
4 communication over the ~~serial~~ ~~PCI-Express-compatible~~ interconnect to the
5 hardware encryption circuit such that the ~~multimedia~~ data output by the logic block
6 is encrypted prior to communication over the ~~serial~~ ~~PCI-Express-compatible~~
7 interconnect.

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1 5. (Currently Amended) The ~~circuit arrangement~~ ~~system~~ of claim 4, wherein the
2 ~~first~~ logic block is ~~additionally configured to output~~ ~~outputs~~ additional data for

3 | communication over an the unencrypted default virtual channel among the
4 | plurality of virtual channels.

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2 | 6. (Currently Amended) The circuit arrangement system of claim 4, wherein the
3 | logic block is configured to output outputs data over the serial PCI-Express
3 | compatible interconnect solely over the dedicated encrypted virtual channel.

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2 | 7. (Currently Amended) The circuit arrangement system of claim 4, further
3 | comprising: wherein the [[a]] second logic block coupled to the multi-channel serial
3 | interface circuit and configured to output outputs data for communication over an
4 | the unencrypted default virtual channel among the plurality of virtual channels.

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2 | 8. (Currently Amended) The circuit arrangement system of claim 4, further
3 | comprising: wherein the [[a]] second logic block coupled to the hardware encryption
3 | circuit and configured to output outputs data for communication over the dedicated
4 | encrypted virtual channel.

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2 | 9. (Currently Amended) The circuit arrangement system of claim 4, further
3 | comprising: wherein the [[a]] hardware decryption circuit coupled intermediate the
3 | multi-channel serial interface circuit and the logic block, the hardware decryption

4 circuit configured to decrypt decrypts encrypted data received from the serial
5 interconnect by the multi channel serial interface circuit and communicated over
6 the dedicated encrypted virtual channel.

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2 10. (Currently Amended) The circuit arrangement system of claim 4, wherein the
3 plurality of virtual channels includes a unencrypted default virtual channel
4 configured to communicate communicates authorization data for authorizing to
authorize secure communication over the dedicated encrypted virtual channel.

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2 11-22. (Canceled)

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2 23. (Currently Amended) A method of providing access control for a digital
3 multimedia data stream, the method comprising:

4 demodulating an encoded multimedia signal to generate a first encrypted
data stream;

5 decrypting the [[a]] first encrypted data stream in a first integrated circuit to
6 generate a first decrypted data stream;

7 re-encrypting the first decrypted data stream in the first integrated circuit to
8 generate a second encrypted data stream;

9 communicating the second encrypted data stream from the first integrated
10 circuit to a second integrated circuit over a ~~multi-channel serial interconnect~~ PCI-
11 Express-compatible interface to which the first and second integrated circuits are
12 connected by communicating the second encrypted data stream over a dedicated
13 encrypted virtual channel, among a plurality of virtual channels, the plurality of
14 virtual channels comprising at least an unencrypted default virtual channel and a
15 dedicated encrypted virtual channel, supported by ~~the multi-channel serial~~ a PCI-
16 Express-compatible interconnect, wherein all data sent over the dedicated
17 encrypted virtual channel are encrypted and wherein access control[[],] and
18 decoding are performed separately on the first and second integrated circuits for the
19 dedicated encrypted virtual channel; and

20 decrypting the second encrypted data stream in the second integrated circuit
21 to generate a second decrypted data stream; and
22 decoding the second decrypted data stream to provide the multimedia signal
23 to a subscriber authorized by the access control.

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1 24-25. (Canceled).

1 26. (Currently Amended) The method of ~~claim 24~~ claim 23, further comprising:

2 performing MPEG decoding on the second decrypted data stream, wherein
3 | the ~~modulated input~~ multimedia signal comprises a satellite broadcast signal, and
4 wherein the first encrypted data stream comprises an encrypted MPEG data
5 stream.

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1 27. (Previously Presented) The method of claim 23, further comprising:
2 performing regional access control on the first encrypted data stream.

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1 28. (Previously Presented) The method of claim 23, further comprising:
2 performing subscriber access control on the first encrypted data stream.

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1 29. (Previously Presented) The method of claim 23, further comprising:
2 disposing the first and second integrated circuits in a set top box.

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1 30. (Previously Presented) The method of claim 23, further comprising:
2 disposing the first integrated circuit on an access card coupled to the second
3 integrated circuit via a connector.

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1 31. (Previously Presented) The method of claim 23, further comprising:

2 performing re-encryption of the first decrypted data stream with hardware
3 encryption logic disposed on the first integrated circuit.

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2 32. (Currently Amended) A-circuit arrangement receiver circuit, comprising:
3 demodulation logic generating a first encrypted data stream from an encoded
4 multimedia signal;
5 first decryption logic configured to perform access control, and to decrypt the
6 [[a]] first encrypted data stream and to generate a first decrypted data stream, the
7 first decryption logic disposed on a first integrated circuit in a processor chip set;
8 encryption logic configured to re-encrypt the first decrypted data stream and
9 generate therefrom a second encrypted data stream;
10 second decryption logic decrypting the second encrypted data stream and
11 generating a second decrypted data stream;
12 decoder logic on a second integrated circuit in the processor chip set, the
13 decoder logic decoding the second decrypted data stream to provide the multimedia
14 signal to a subscriber authorized by the access control; and
15 a multi-channel serial first PCI-Express-compatible interface circuit configured
16 to communicate communicating the first and the second encrypted data
17 stream over a multi-channel serial PCI-Express-compatible interconnect by
 communicating the second encrypted data stream over a dedicated encrypted

18 virtual channel, among a plurality of virtual channels, the plurality of virtual
19 channels comprising at least an unencrypted default virtual channel and a
20 dedicated encrypted virtual channel, supported by the multi-channel serial
21 interconnect, wherein all data sent over the dedicated encrypted virtual channel are
22 encrypted, and wherein access control[[,]] and decoding are performed separately on
23 the first and second integrated circuits for the dedicated encrypted virtual channel.

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1 33-35. (Canceled).

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1 36. (Currently Amended) The-circuit arrangement of claim-35 receiver circuit of
2 claim 32, wherein the modulated input encoded multimedia signal comprises a
3 satellite broadcast signal, wherein the first encrypted data stream comprises an
4 encrypted MPEG data stream, and wherein decoding the second decrypted data
5 stream in the second integrated circuit comprises performing MPEG decoding on
6 the second decrypted data stream.

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1 37. (Currently Amended) The-circuit arrangement of claim-35 receiver circuit of
2 claim 32, wherein the demodulation logic, the encryption logic, and the multi-
3 channel serial first PCI-Express-compatible interface circuit are disposed on the
4 first integrated circuit, wherein the second decryption logic is disposed on the

5 second integrated circuit, and wherein the second integrated circuit includes a
6 second ~~multi-channel serial~~ PCI-Express-compatible interface circuit coupled to the
7 ~~multi-channel serial~~ PCI-Express-compatible interconnect to receive the second
8 encrypted data stream.

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2 38. (Currently Amended) ~~The circuit arrangement of claim 32 receiver circuit of~~
3 claim 32, wherein the first decryption logic performs regional access control on the
first encrypted data stream.

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2 39. (Currently Amended) ~~The circuit arrangement of claim 32 receiver circuit of~~
3 claim 32, wherein the first decryption logic performs subscriber access control on
the first encrypted data stream.

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40-45. (Canceled)